**GUIDELINES of B.Sc. (H) COMPUTER SCIENCE**

**(Under Choice Based Credit System Scheme)**

**Semester I**

**Core Course – II**

**COMPUTER SYSTEM ARCHITECTURE**

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| **S. No.** | **Chapter Number and Name** | **Section Numbers** | **No. of Lectures\*** | **Chapter wise Weightage\***  **(Marks)** |
| 1 | Ch 1:  Digital Logic Circuits | 1.1 - 1.3, 1.4 (up to three variable K-map),  1.5 ,  1.6 (up to pg. 25),  1.7 (up to pg. 28) | 10 | 10 |
| 2 | Ch 2:  Digital Components | 2.2 (up to pg. 44 including Table 2.1),  2.3 (up to pg. 49),  2.7 | 4 | 4 |
| 3 | Ch 3:  Data Representation | 3.1 – 3.4 | 8 | 8 |
| 4 | Ch 5:  Basic Computer Organization and Design | 5.1 – 5.3,  5.4 (up to pg. 137),  5.5 – 5.8,  5.9 (up to pg. 159) | 16 | 16 |
| 5 | Ch 6:  Programming the Basic Computer | 6.1 | 1 |
| 6 | Ch 8:  Central Processing Unit | 8.1 – 8.2,  8.3 (up to pg. 247),  8.5,  8.8 (only characteristics, i.e., pg. 282 – 284) | 6 | 10 |
| 7 | Ch 9:  Pipeline and Vector Processing | 9.1 – 9.2 | 4 | 6 |
| 8 | Ch 10:  Computer Arithmetic | 10.3 (pg. 343 – 346, i.e., Booth Multiplication Algorithm),  10.4 (pg. 349, without hardware implementation) | 3 | 5 |
| 9 | Ch 11:  Input Output Organization | 11.1 (up to pg. 383),  11.2 (up to pg. 389, excluding example),  11.4,  11.6,  11.7 (up to pg. 421) | 4 | 8 |
| 10 | Ch 12:  Memory Organization | 12. 4 (up to pg. 458),  12.5 | 4 | 8 |

\*The number of lectures and chapter wise weightage may be treated as indicative only.

**Reference:**

Computer System Architecture: Morris M. Mano (Pearson Education, 3rd Edition, 2004 Reprint)